WHAT IS CLAIMED IS

1. A thin-film circuit substrate, comprising:

a semiconductor substrate having a first principal plane and a second principal plane that counters the first principal plane,

a first insulator layer formed on the first principal plane of the semiconductor substrate,

a through hole that continuously extends from the second principal plane to the first principal plane through the inside the semiconductor substrate, including a main section substantially having a first diameter and extending from the second principal plane, and a tapered section having a second diameter that is larger than the first diameter near the first principal plane,

a second insulator layer that covers a side wall face of the through holes, and

a thin-film circuit formed on the first insulator layer.

2. The thin-film circuit substrate as claimed in claim 1, wherein the first insulator layer is provided with an opening formed by an inner wall surface of the second insulator layer of the through holes.

3. The thin-film circuit substrate as claimed in claim 2, wherein the first insulator layer has an extension part extending at the opening toward a center of the opening beyond the sidewall of the through hole at a distance corresponding to a thickness of the second insulator layer, the extension part being defined by a sidewall surface coincident with the first principal plane and an end surface coincident with the opening, the second insulator layer engaging with the sidewall surface of the extension part.

4. The thin-film circuit as claimed in claim 1, wherein a side of the thin-film circuit substrate, which contacts the first insulation layer, is a flat face.

5. The thin-film circuit substrate as claimed in claim 2, wherein a concavity of a diameter larger than the opening on a side that touches the first insulator layer, corresponding to the through hole, is provided.

6. The thin-film circuit substrate as claimed in claim 2, wherein an insulator layer pattern that has a diameter larger than the openings, corresponding to the through hole, is provided between the thin-film circuit and the first

insulator layer.

7. The thin-film circuit substrate as claimed in claim 1, wherein a thickness of the second insulator layer is larger than a thickness of the first insulator layer.

8. The thin-film circuit substrate as claimed in claim 1, wherein the through hole is filled with an electrically conductive material.

9. The thin-film circuit substrate as claimed in claim 1, further comprising a ferroelectric film or a high dielectric film.

10. The thin-film circuit substrate as claimed in claim 1, wherein the first insulator layer and the second insulator layer are an oxide film.

11. A manufacturing method of a thin-film circuit substrate, comprising:

a step of forming an etching stop film on a first principal plane of a semiconductor substrate having the first principal plane and a second principal plane,

a step of forming a resist pattern that has a resist opening on the second principal plane of the semiconductor substrate,

a step of forming a hole through the semiconductor substrate corresponding to the resist opening by applying dry etching to the semiconductor substrate using the resist pattern as a mask such that the etching stop film is exposed in the through holes,

a step of forming an insulator layer on a side wall face of the through holes,

a step of forming a thin film circuit on the etching stop film, and

a step of forming an opening by removing the etching stop film at the through hole such that the thin film circuit is exposed.

12. The manufacturing method of the thin-film circuit substrate as claimed in claim 11, wherein the dry etching is further continued after the etching stop film is exposed such that an over-etching is performed.

13. The manufacturing method of the thin-film circuit substrate as claimed in claim 12, wherein the step of forming the etching stop film includes a step of forming an insulation film

pattern that covers a formation area of the through hole on the first principal plane as the etching stop film on the first principal plane, and a step of forming an oxide film around the insulator film pattern by oxidizing the first principal plane of the semiconductor substrate, using the insulator film pattern as a mask, wherein the oxide film functions as an over-etching stop film in the step of over-etching.

14. The manufacturing method of a thin-film circuit substrate as claimed in claim 11, wherein the etching stop film is made of SiN or SiO_2.

15. The manufacturing method of a thin-film circuit substrate as claimed in claim 11, wherein the thin-film circuit includes a ferroelectric film or a high dielectric film, and the step of forming the thin-film circuit includes a step of a heat treatment in an oxidization atmosphere.

16. The manufacturing method of a thin-film circuit substrate as claimed in claim 11, further comprising a step of filling the through hole with a conductive material after the step of removing the etching stop film is finished.

17. A via formed substrate, comprising:

a supporting substrate having a first principal plane and a second principal plane that counters the first principal plane,

a through hole having a first diameter, extending from the second principal plane toward the first principal plane through the supporting substrate,

a taper form section that is formed in an edge section on the first principal plane side of the through holes, having an opening in the first principal plane, with a diameter increasing from the first diameter toward the first principal plane until the diameter measured at the first principal plane reaches a second diameter that is larger than the first diameter,

a plug that is electrically conductive for filling the through holes, and

an electrode pad having a taper form corresponding to the taper form section, electrically connected to the plug.

18. The via formed substrate as claimed in claim 17, further comprising a vamp electrode on the electrode pad.

19. The via formed substrate as claimed in claim 17, wherein the supporting substrate is made

of Si.

20. The via formed substrate as claimed in claim 19, wherein the taper form section is formed on an Si crystal face.

21. The via formed substrate as claimed in claim 17, wherein the second diameter is greater than twice as large as the first diameter.

22. The via formed substrate as claimed in claim 17, wherein a thin-film circuit is formed on the supporting substrate.

23. A manufacturing method of a via formed substrate, comprising:

a step of forming a tapered concavity by anisotropic etching on a first principal plane of a semiconductor substrate,

a step of forming an insulation layer in a form corresponding to the tapered concavity, covering the surface of the tapered concavity,

a step of forming such that a via hole that extends from a second principal plane that counters the first principal plane toward the first

principal plane of the semiconductor substrate exposes the insulation layer at the tapered concavity corresponding to the tapered concavity,

a step of forming an electrode pad on the insulation layer that cover the tapered concavity in a shape corresponding to a top part of the tapered concavity,

a step of removing the insulator layer at a bottom part of the via hole such that the electrode pad is exposed, and

a step of forming a via plug by filling the via hole with an electrically conductive material.

24. The manufacturing method of the via formed substrate as claimed in claim 23, wherein the semiconductor substrate is made of Si, and the anisotropic etching process is performed by wet etching.

25. The manufacturing method of the via formed substrate as claimed in claim 23, wherein the via hole is formed by dry etching.

26. The manufacturing method of the via formed substrate as claimed in claim 23, wherein the step of forming the via plug includes a plating process of the electrically conductive material.

27. The manufacturing method of the via formed substrate as claimed in claim 23, wherein the electrically conductive material is one of Pt and Au.

28. The manufacturing method of the via formed substrate as claimed in claim 23, further comprising:

a step of forming soldering paste on the electrode pad, and

a step of preparing a solder ball on the soldering paste corresponding to the electrode pad.

29. The manufacturing method of the via formed substrate as claimed in claim 28, further comprising a step of forming a vamp electrode on the electrode pad by applying heat to the solder ball.